

REMARKS

This Amendment is filed in response to the Advisory Action dated October 2, 2003, which has a shortened statutory period set to expire November 12, 2003.

Applicants herein submit a Request For Continuing Examination (RCE) with a Request For Extension Of Time. This response to the Advisory Action cancels all previously pending Claims 1-36 and adds new Claims 37-58.

Applicants respectfully submit that Claims 37-58 are patentable over the cited art. Specifically, Claim 37 recites that a memory model includes:

- a plurality of primitives including a memory primitive;
- a read data port primitive for coupling to an output port of the memory primitive;
- an address bus primitive for coupling to the memory primitive and the read data port primitive;
- a data bus primitive for coupling to the memory primitive; and
- a plurality of memory out primitives.

In contrast, Beausang teaches a circuit model 300 (Fig. 3A) that includes a memory cell block and combinational logic. Col. 9, lines 29-33. Beausang further teaches a technology independent netlist that is composed of logical primitives and operators of the IC layout, but the components described therein contain no structure. Col. 14, lines 39-42. However, Beausang teaches nothing regarding a memory model, much less a memory model comprising a plurality of primitives.

Cheng fails to remedy the deficiencies of Beausang. Specifically, Cheng provides a survey of methods and techniques for sequential circuit test generation for single stuck-at faults. Page 406. In particular, Cheng focuses on the methods

based on gate-level circuit models. Page 406. Cheng fails to teach anything regarding a memory, much less a memory model.

Because Beausang and Cheng fail to disclose or suggest the recited primitives comprising the memory model, Applicants request allowance of Claim 37.

Claims 38-50 depend from Claim 37 and therefore are patentable for at least the reasons presented for Claim 37. Moreover, Claims 38-50 recite further limitations regarding each of the primitives that are neither disclosed nor suggested by Beausang and Cheng. Therefore, Applicants request allowance of Claims 38-50.

Claim 51 recites that a content addressable memory (CAM) model includes:

- a memory primitive;
- a compare port primitive for coupling to an output port of the memory primitive;
- an address bus primitive for coupling to the memory primitive and the compare port primitive;
- a data bus primitive for coupling to the memory primitive; and
- a plurality of memory output primitives, each memory output primitive for coupling to the compare port primitive.

Applicants respectfully submit that Beausang and Cheng fail to disclose or suggest this CAM model for substantially the same reasons presented for Claim 37. Based on those reasons, Applicants request allowance of Claim 51.

Claim 52 depends from Claim 51 and therefore is patentable for at least the reasons presented for Claim 51. Moreover, Claim 52 recites further limitations regarding the compare port

primitive that is neither disclosed nor suggested by Beausang and Cheng. Therefore, Applicants request allowance of Claim 52.

Claim 53 recites a combined content addressable memory (CAM) and random access memory (RAM) model that includes:

- a first memory primitive;
- a data bus primitive;
- a compare port primitive for coupling to the memory primitive and the data bus primitive;
- a plurality of memory output primitives, each memory output primitive for coupling to the compare port primitive;
- an address bus primitive for coupling to a first subset of the plurality of memory output primitives;
- a second memory primitive;
- a read data port primitive for coupling to the second memory primitive, the address bus primitive, and a second subset of the plurality of memory output primitives; and
- a plurality of memory output primitives, each memory output primitive for coupling to the read data port primitive.

Applicants respectfully submit that Beausang and Cheng fail to disclose or suggest this CAM-RAM model for substantially the same reasons presented for Claim 37. Based on those reasons, Applicants request allowance of Claim 53.

Claim 54 depends from Claim 53 and therefore is patentable for at least the reasons presented for Claim 53. Moreover, Claim 54 recites further limitations regarding the compare port primitive that is neither disclosed nor suggested by Beausang and Cheng. Therefore, Applicants request allowance of Claim 54.

Claim 55 recites a memory model that is compatible with a simulation tool and an automatic test pattern generation (ATPG) tool. The memory model includes:

a plurality of primitives, each primitive representing a defined functionality of a memory.

Applicants respectfully submit that Beausang and Cheng fail to disclose or suggest this memory model for substantially the same reasons presented for Claim 37. Based on those reasons, Applicants request allowance of Claim 55.

Claims 56-58 depend from Claim 55 and therefore are patentable for at least the reasons presented for Claim 55. Moreover, Claims 56 and 58 recite further limitations regarding the memory model that are neither disclosed nor suggested by Beausang and Cheng. Therefore, Applicants request allowance of Claims 56-58.

Applicants' recited memory models have significant advantages. For example, Applicants' recited memory models can be constructed directly from behavioral descriptions. Thus, the tedious, time-consuming, error-prone, and difficult tasks of manually re-coding ATPG models for memories and verifying functional equivalence between simulation models and ATPG models can be eliminated. Specification, page 5, lines 6-11. Moreover, such memory models can be easily debugged using a schematic viewer. Specification, page 6, lines 15-20. These advantages cannot be achieved using the teachings of the cited art.


CONCLUSION

Claims 37-58 are pending in the present application.
Applicants request allowance of these claims.

If there next action is other than allowance, please
telephone the undersigned at 408-451-5907 to schedule a
telephone interview.

Respectfully submitted,

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